Atty. Dkt. No.: 39153/484 (G1190)

U.S. PATENT APPLICATION

for

METHOD OF USING AN ADHESION PRECURSOR LAYER FOR CHEMICAL VAPOR DEPOSITION (CVD) COPPER DEPOSITION

Inventors: Sergey D. Lopatin
Paul R. Besser
Alline F. Myers
Jeremias D. Romero
Minh Q. Tran
Lu You
Pin-Chin Connie Wang

METHOD OF USING AN ADHESION PRECURSOR LAYER FOR CHEMICAL VAPOR DEPOSITION (CVD) COPPER DEPOSITION

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is related to U.S. Patent Application No. 10/145,944, Attorney Docket No. 39153/452 (G1157), entitled METHOD OF FORMING AN ADHESION LAYER WITH AN ELEMENT REACTIVE WITH A BARRIER LAYER, assigned to the same assignee as this application.

FIELD OF THE INVENTION

[0002] The present invention relates generally to integrated circuits and methods of manufacturing integrated circuits. More particularly, the present invention relates to using an adhesion precursor layer for chemical vapor deposition (CVD) copper deposition.

BACKGROUND OF THE INVENTION

[0003] Semiconductor devices or integrated circuits (ICs) can include millions of devices, such as, transistors. Ultra-large scale integrated (ULSI) circuits can include complementary metal oxide semiconductor (CMOS) field effect transistors (FET). Despite the ability of conventional systems and processes to fabricate millions of IC devices on an IC, there is still a need to decrease the size of IC device features, and, thus, increase the number of devices on an IC. Nevertheless, there are many factors that make the continued miniaturization of ICs difficult. For example, as the size of vias (or pathways between integrated circuit

layers used to electrically connect separate conductive layers) decreases, electrical resistance increases.

[0004] Conventional integrated circuits utilize vias to connect structures (e.g., gates, drain regions, source regions) and conductive lines. For example, a via can connect a gate above the substrate to a conductor line in a metal 1 layer. Vias can also interconnect conductive lines. For example, a via can connect a conductive line in a metal 1 layer to a conductor line in a metal 2 layer. A via is typically a metal plug which extends through an insulative layer in a multilayer integrated circuit. Vias and barrier layers are discussed in U.S. Patent Nos. 5,646,448; 5,770,519; and 5,639,691; each of which are assigned to the assignee of the present application.

[0005] A barrier layer is used to protect the via and insulative layer from metal diffusion and the via and conductive line from electromigration (EM). The barrier layer can contribute significantly to resistance associated with the via metal. Electromigration is the mass transport due to momentum exchange between conducting electrons and diffusing metal atoms. Electromigration causes progressive damage to the metal conductors in an integrated circuit. In general, metals are most susceptible to electromigration at very high current density and temperatures of 100° C or more.

[0006] According to a conventional plasma vapor deposition (PVD) process, IC manufacturers deposit a very thin barrier layer of Tungsten (W). The barrier layer can be deposited in a SiH_4, WFl_6 → WSi_2 process. The barrier layer servers to adhere to the underlying dielectric layer and serve as a nucleation layer to further Tungsten deposition. Additional layers of Tungsten can be deposited in a WFl_6 + H_2 deposition process without the use of SiH_4.

[0007] Other conventional conductive lines have utilized pure copper or copper alloy lines formed in a damascene process. According to a conventional damascene process, copper lines are filled by electroplating a trench in a dielectric layer. The dielectric layer is typically covered by a barrier and/or a seed layer before electroplating to fill the trench with copper. After the trench is filled with copper, a barrier layer is provided above a copper conductive line and a subsequent interlevel dielectric layer is provided. The barrier layer is necessary to prevent electromigration and to protect the dielectric layer from copper diffusion. Further, the barrier layer reduces problems associated with having the dielectric material adhere to dielectric material.

[0008] Forming continuous barrier layers in ultra-narrow vias and metal lines can be difficult. Vias and trenches for the metal lines can be less than 160 nm in width, making formation of continuous and conformal barrier and/or seed layers challenging. As IC fabrication techniques improve, the via and trench widths become ever smaller. Therefore, metallization of in-laid trenches and vias is becoming a more difficult task.

[0009] Thus, there is a need for method of using an adhesion precursor for chemical vapor deposition (CVD) copper deposition. Further, there is a need for a method of causing copper to better adhere to dielectric material to form a continuous barrier layer in vias and metal lines. Even further, there is a need for an improved electromigration barrier.

SUMMARY OF THE INVENTION

[0010] An exemplary embodiment is related to a method of using an adhesion precursor in an integrated circuit fabrication process.

The method includes providing a gas of material over a dielectric material and providing a copper layer over an adhesion precursor layer. The adhesion precursor layer is formed by the gas, and the dielectric material includes an aperture.

[0011] Another exemplary embodiment is related to a method of improving adhesion between a copper layer and a dielectric layer by providing an adhesion precursor. The method includes forming a trench in a dielectric layer, providing an adhesion precursor gas above the dielectric layer and the trench to form an adhesion precursor layer, providing an alloy layer above the adhesion precursor layer, and providing a copper layer above the alloy layer.

[0012] Another exemplary embodiment is related to a method of using an adhesion precursor for chemical vapor deposition. The method includes forming a trench in a dielectric layer, forming a continuous barrier layer above the dielectric layer and along sides of the trench, depositing copper above the continuous barrier layer where the copper located in the trench forms an integrated circuit feature.

[0013] Other principle features and advantages of the invention will become apparent to those skilled in the art upon review of the following drawings, the detailed description, and the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] The exemplary embodiments will hereafter be described with reference to the accompanying drawings, wherein like numerals denote like elements, and:

[0015] FIGURE 1 is a flow diagram depicting exemplary operations in a process for using an adhesion precursor in an integrated circuit fabrication process in accordance with an exemplary embodiment;

[0016] FIGURE 2 is a schematic cross-sectional view representation of a portion of an integrated circuit, showing a barrier adhesion layer formation in accordance with an exemplary embodiment;

[0017] FIGURE 3 is a schematic cross-sectional view representation of a portion of an integrated circuit, showing gas deposition in accordance with another exemplary embodiment;

[0018] FIGURE 4 is a schematic cross-sectional view representation of a portion of an integrated circuit, showing a bulk deposition in accordance with an exemplary embodiment; and

[0019] FIGURE 5 is a schematic cross-sectional view representation of a portion of an integrated circuit, showing a copper via over a barrier adhesion layer in accordance with another exemplary embodiment.

DETAILED DESCRIPTION OF THE EXEMPLARY EMBODIMENTS

[0020] With reference to FIGURE 1, an advantageous process 10 for forming a conductive line that allows copper deposited with suitable adhesion is disclosed. Process 10 utilizes a layered conductive line structure.

[0021] Process 10 includes a dielectric layer formation operation 12, a trench formation operation 14, a adhesion precursor operation 16 and a conductive layer formation step 18. In dielectric layer formation operation 12, a dielectric material is provided above a substrate

or other underlying layer. The dielectric material can be deposited using a variety of techniques, including chemical vapor deposition. In trench formation operation 14, a trench or an aperture is formed in the dielectric material layer formed in dielectric layer formation operation 12. A trench can be formed using an etching technique, such as reactive ion etching (RIE) or plasma etching.

[0022] In adhesion precursor operation 15, an adhesion precursor layer is provided above the dielectric layer, including side walls of the dielectric layer defined by the trench formed in the dielectric layer. The adhesion precursor can be provided as a gas in some type of vapor deposition process. The adhesion precursor gas forms a layer that helps improve adhesion between the dielectric material and the conductive line.

[0023] In conductive layer formation operation 18, a conductive layer is provided above the adhesion precursor layer. A variety of different deposition techniques may be used to provide the conductive material that makes up the conductive layer. For example, a plasma enhanced chemical vapor deposition (PECVD) can be used. Conductive material formed in the trench can be used as an interconnect or via.

[0024] With reference to FIGURE 2, a schematic cross-sectional view representation of a portion 100 of an integrated circuit includes an aperture 105 and a dielectric layer 115. Portion 100 is preferably part of an ultra- large-scale integrated (ULSI) circuit having millions or more transistors. Portion 100 is manufactured as part of the integrated circuit on a semiconductor wafer, such as, a silicon wafer.

[0025] Aperture 105 is formed in preparation for the creation of a via or trench by etching a portion of dielectric layer 115. In an exemplary embodiment, dielectric layer 115 is an oxide material or

other suitable material. Layer 115 can be provided above another dielectric layer or a substrate.

[0026] A gas 108 including an initial depositing metal is provided to portion 100. Gas 108 is selected to include materials that form a thin barrier adhesion layer conformal to side walls of aperture 105 and a top 111 of dielectric layer 115. Gas 108 can include tantalum nitride (TaN), tungsten nitride(WN), disilicon nitride (Si_2N), or any of a variety of other barrier materials. Preferably, gas 108 deposits a layer with a cross-sectional thickness of up to 500 Angstroms.

[0027] FIGURE 3 illustrates portion 100 after formation of a barrier adhesion layer 120. Barrier adhesion layer 120 can have a thickness of 10 to 100 Angstroms. Advantageously, barrier adhesion layer 120 is a thin, continuous, and controllable layer that is adhesive to copper. Barrier adhesion layer 120 can help prevent electromigration effects. Further, barrier adhesion layer 120 adheres to dielectric layer 115.

[0028] In at least one exemplary embodiment, barrier adhesion layer 120 can include a ternary element, such as, Iridium (Ir), Ruthenium (Ru), Rhenium (Re), or other suitable material. The alloy element for barrier adhesion layer 120 can be applied at a dose of $2e^{14}$atoms/cm^2 or $2e^{15}$atoms/cm^2 and applied at an energy of, for example, 0.5 to 5 keV.

[0029] In at least one embodiment, a gas 123 can be provided to deposit an initial material over barrier adhesion layer 120. Gas 123 can include a material, such as, zirconium (Zr), calcium (Ca), or aluminum (Al). Preferably, gas 123 has a concentration of 30% of the material. A gas 125 can also be provided over barrier adhesion layer 120. Gas 125 can include copper (Cu) at a concentration of 10%.

[0030] In at least one alternative embodiment, a gas 127 can be provided in addition to gases 123 and 125. Gas 127 can include an alloying element. The alloying element of gas 127 can include tin(Sn), indium (In), zinc (Zn), or chromium (Cr). The alloying element can be chosen to improve electromigration effects.

[0031] FIGURE 4 illustrates portion 100 after the gases 123 and 125 are provided. In at least one embodiment, gas 127 is also provided. The deposited gases can form a blending layer 133 conformal to barrier adhesion layer 120. Blending layer 133 can be up to 250 Angstroms in thickness.

[0032] A gas 135 can be provided over blending layer 133 and barrier adhesion layer 120. Gas 135 can include materials for a bulk deposition of, for example, copper (Cu). In an exemplary embodiment, gas 135 has a concentration of 30% of Cu. In at least one alternative embodiment, a gas 137 including an alloying element is also provided. Alloying elements in gas 137 can be zirconium (Zr), calcium (Ca), aluminum (Al), lanthanum (La), or hafnium (Hf).

[0033] FIGURE 5 illustrates portion 100 after formation of a copper layer 140, an alloy layer 150, a copper layer 155, and a barrier 160. Copper layer 140 and copper layer 155 can be formed by materials contained in gas 135 described with reference to FIGURE 3. Alloy layer 150 can be formed by materials contained in gas 137 described with reference to FIGURE 4.

[0034] Copper layer 140 can have a thickness of up to 5,000 Angstroms. Alloy layer 150 can have a thickness of up to 50 Angstroms. Barrier 160 can be formed at the top of copper layer 155. Barrier 160 can be located where a chemical mechanical polish (CMP) is expected to stop. As such, barrier 160 can provide an anti-dishing layer.

[0035] Alloy layer 150 can be provided between copper layer 140 and copper layer 155 at a location just below an exposed post-CMP surface to help preserve an upper interface from copper electromigration. Therefore, portion 100 can be planarized until layer 150 is reached. In FIGURE 5, layer 150 is not located above layer 155.

[0036] Advantageously, use of an adhesion precursor layer, such as, barrier adhesion layer 120, allows the formation of a continuous barrier layer in ultra-narrow vias and metal lines. Use of chemical vapor deposition (CVD) in creation of various layers described with reference to the FIGURES can provide better step coverage as well as controlled atomic layer thickness of deposited layers.

[0037] While the exemplary embodiments illustrated in the figures and described above are presently preferred, it should be understood that these embodiments are offered by way of example only. Other embodiments may include, for example, different gases, concentrations of materials, and alloying elements. The invention is not limited to a particular embodiment, but extends to various modifications, combinations, and permutations that nevertheless fall within the scope and spirit of the appended claims.